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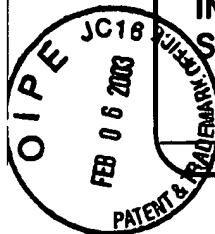
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 1

Complete If Known

Application Number	09/955,693
Filing Date	September 18, 2001
First Named Inventor	Cao, Jun
Art Unit	2634
Examiner Name	Stephen Chin
Attorney Docket Number	019717-002700US

**U.S. PATENT DOCUMENTS**

Examiner	Cite No. ¹	Document Number Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
LW	AA	US-6,121,804	09-19-2000	Bryan et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ Number ⁴ Kind Code ⁵ (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
LW	AB	PCT	WO 01/06696	01-25-2001	Chang et al.		<input type="checkbox"/>
LW	AC	PCT	WO 01/63767	08-30-2001	Green		<input type="checkbox"/>

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
LW	AD	CHARLES R. HOGGE, JR., "A Self Correcting Clock Recovery Circuit", Journal of Lightwave Technology, Vol. LT-3, No. 6, December 1985 (Previously cited in IDS filed July 9, 2002)	

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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Approved for use through 10/31/2002. OMB 0651-0031

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LW	AA	US-4,535,459	08-13-1985	Hogge, Jr.	
LW	AB	US-5,301,198	04-05-1994	Ewen et al.	
LW	AC	US-09/784,419	filed 02-15-2001	Jun Cao	

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	AD					
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LW	AF	C.R. HOGGE "A self-correcting Clock Recovery Circuit", IEEE Journal of Lightwave Technology, vol. LT-3, pp. 1312-1314, Dec. 1985	
LW	AG	E. MULLNER, "A 20 Gb/s Parallel Phase Detector and Demultiplexer Circuit in a Production Silicon Bipolar Technology with $f_T=25$ GHz", Proc. IEEE BCTM, pp. 43-45, Oct. 1996	
LW	AH	M. RAU et al., "Clock/Data Recovery PLL Using Half-Frequency Clock", IEEE Journal of Solid-State Circuits, vol. 32, no. 7, July 1997	
LW	AI	K. NAKAMURA et al., "A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock", IEEE, 1998 Symposium on VLSI Circuits Digest of Technical Papers	
	AJ	M. WURZER et al., "40 Gb/s Integrated Clock and Data Recovery Circuit in a Silicon Bipolar Technology", IEEE, 1998	
LW	AK	JAFAR SAVOJ et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit", IEEE, 2000 Symposium on VLSI Circuits Digest of Technical Papers	

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